DRAW

Fig. 1 -- Signal Flow Driven Circuit Analysis and Partition Flow Chart

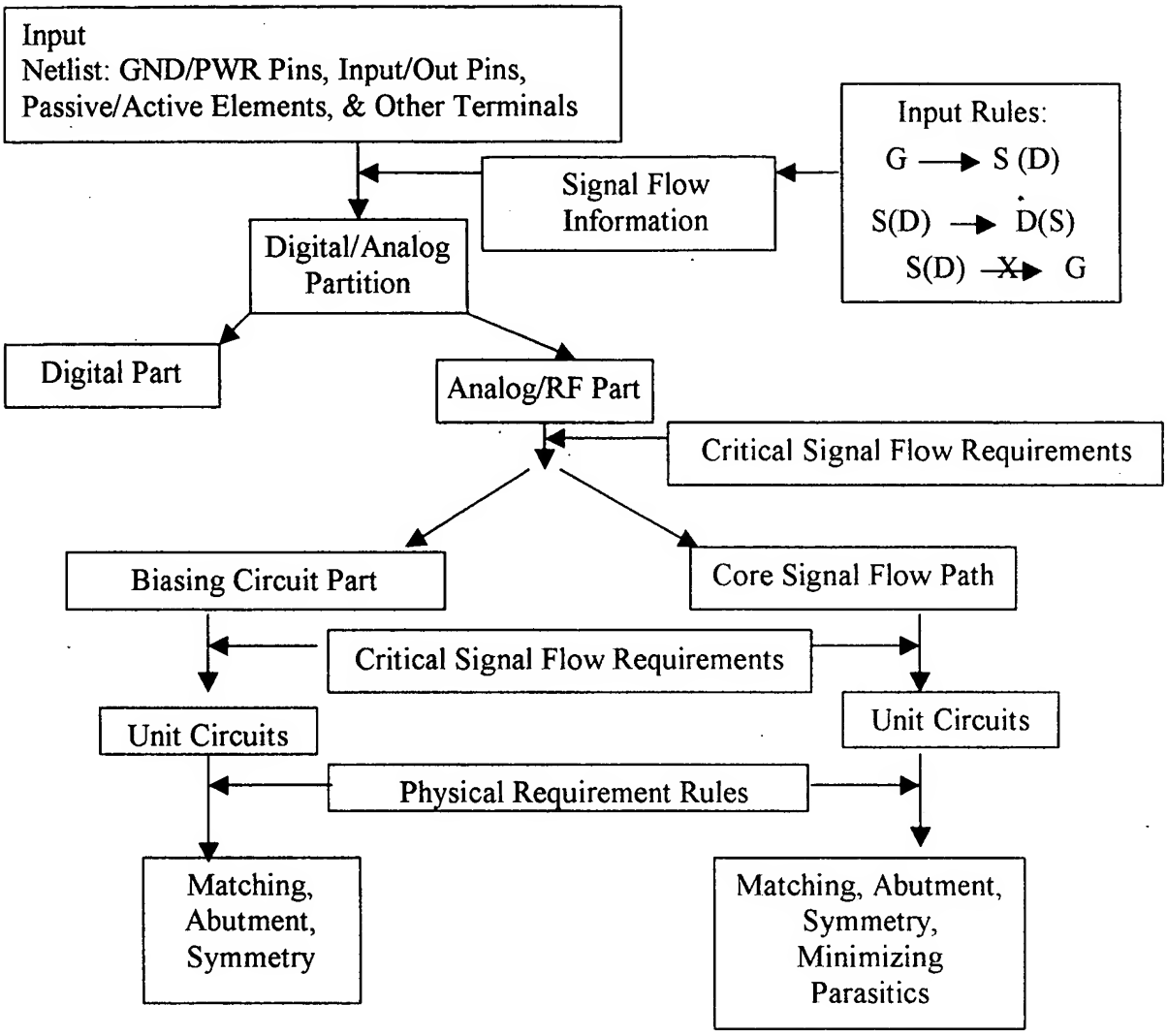

Fig. 2 – Means of Circuit Performance Assessment and Circuit Yield Enhancement Flow Chart

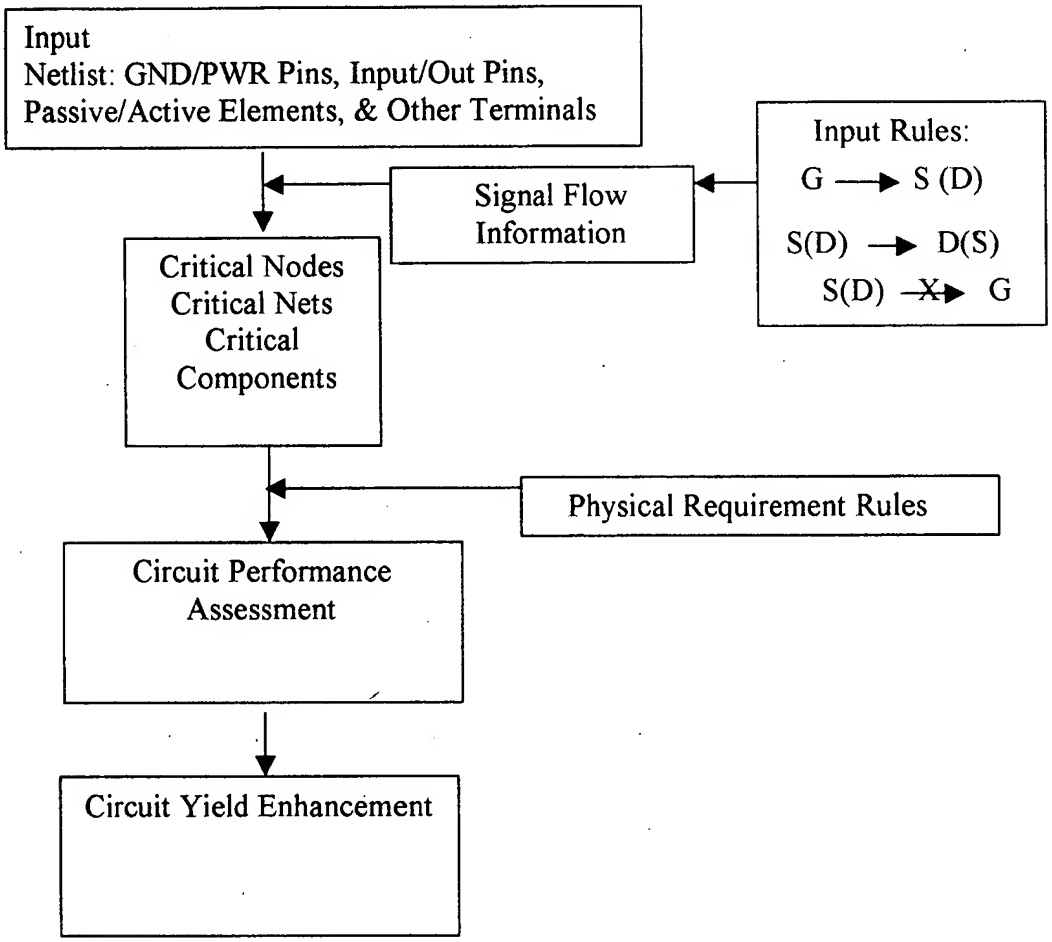

Fig. 3 -- Means of Circuit Hierarchy Regeneration, Performance Optimization, Physical Layout Optimization, Floor Planning, and Extracting Intellectual Property Circuit Cell Flow Chart